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Design and Implementation of RCA and CSA by Using Reconfigurable Adder Architecture

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Abstract: Higher performance, lower cost, increasingly minimizing integrated circuit components, and higher packaging density of chips are ongoing goals of the microelectronics and computer industry. As these goals are being achieved, however, power consumption and flexibility are increasingly becoming bottlenecks that need to be addressed with the new technology in Very Large-Scale Integrated (VLSI) design. Combinational circuits are the heart of electronic devices. Among these combinational circuits the adders are of great importance as these are used at the multiple levels for calculations in functioning of the devices.Coarse-grained reconfigurable architectures (CGRAs) have the potential to offer performance approaching an ASIC with the flexibility, within an application domain, similar to a digital signal processor. In the past, coarse-grained reconfigurable architectures have been encumbered by challenging programming models that are either too farremoved from the hardware to offer reasonable performance or bury the programmer in the minutiae of hardware specification.Theproposed architecture enables the designer to perform efficientDesign Space Exploration. The design can be made adaptable toany of the reconfigurable processor and a similar improvement can be obtained.

Keywords: Adders, low power VLSI, verilog, Spartan-III, FPGA.

I. INTRODUCTION

Typical issues for VLSI designers are to reduce thearea of the chip and increase its performance for computational applications like video compression, graphics, gaming consoles etc. But the developmentof portable devices and palm held devices, hasforced the designers to optimize the power consumption of the device while still meeting thecomputational requirements. The wireless devicesare also making their way to the consumer electronics market where the power consumption isthe key design constraint. Hence the powerconsumption of the device needs to be addressed toincrease the run time of the batteries with minimumrequirements on size, durability and weight allocated to it. Absence of low power architectures causes theportable devices to suffer from short battery life or require large battery pack. Increase in powerconsumption in the chips need expensive packaging and cooling devices, and hence it's a clear advantage of cost to go for low power devices.Addition to the cost, high power consumption leadsto the issue of reliability, because the high powerconsumption increases the temperature and it tendsto exacerbate several silicon failure mechanisms. Excessive power consumption limits the integration of more transistors on the single chip oron multichip modules. This is due to the heat generated from power consumption limits the feasible packaging and performance of the VLSI systems. Motivation of reducing power consumption depends on the applications and how much the designer is willing to sacrifice in cost or performance to obtain the low power consumption devices. The designer might sacrifice the performance for extended battery life of the battery powered devices and suppose if both power and performance are important then thepower delay product need to be minimized. Hence in this brief, low power architecture are proposed atcomparable performance or negligible performance constraints for the data path components as they are the repeatedly used blocks in any digital circuits. Arithmetic components are responsible for thecomputations and they are the basic building blocksin intensive computational applications. Among thearithmetic components adders are the essential elements and are used repeatedly in any computational intense applications. This enabled many research organizations towards the development of low power computational architectures. In this brief, an effort has beenattempted to develop low power heterogeneous adder architecture which consume less power and provide delay optimizations.

A. ARCHITECTURES

Ripple Carry Adder consists of cascaded "N" single bitfulladders. Output carry of previous adder becomes the inputcarry of next full adder. Therefore, the carry of this addertraverses longest path called worst case delay path through Nstages. Fig. 1 shows the block diagram of ripple carry adder.Now as the value of N increases, delay of adder will alsoincrease in a linear way. Therefore, RCA has the lowestspeed amongst all the adders because of large propagationdelay but it occupies the least area. Now CSLA provides away to get around this linear dependency is to anticipate allpossible values of input carry i.e. 0 and 1 and evaluate theresult in advance. Once the original value of carry is known,result can be selected using the multiplexer stage. Thereforethe CSLA makes use of Dual RCA's to generate the partialsum and carry by considering input carry Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers.

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Adder is the essential component in any digitalsystem and many variations are introduced in thecarry generation schemes for area, speed and powertrade-offs. Hybrid adders were developed in the pastto provide area and speed trade-off by utilizingdifferent schemes for sum and carry logicseparately. Several homogeneousadders were reconfigured with their bit widths toachieve variable performance and power trade-offs.Architectures reported in have adder variantswhere larger bit system is partitioned in to smallerbits and reconfigured using additional bits. Such addersprovide the selection of the bit widths of the addersand improve efficiency of the design. An effort hasbeen put in to add the extra flexibility into thesystem where different adder variants of smaller bitwidths are incorporated in the larger adder system toaddress the delay optimization under powerconstraints or power optimization under delayconstraints. Such architectures are called asHeterogeneous adders. In this paper, we propose thelow power heterogeneous adder architecture toprovide power optimization with variable performance.

Limitations of the state of the art reconfigurable architectures,

a) In the regular reconfigurable architectures, static/dedicated adder architectures are utilized and multiplexer selects the required adder variant. This requires more area and consumes more power to achieve variable performance and reconfigureability between the adder variants.

b) In the state of the art heterogeneous architecture, the static sub-adder blocks consumes more powerwhile still providing good performance.

In this paper, we address the above limitations:

- Low power adder architecturesComplex cells wereutilized to build theadder architecture, as they eliminate theinterconnect delays between the gatesand helps in reducingpower.

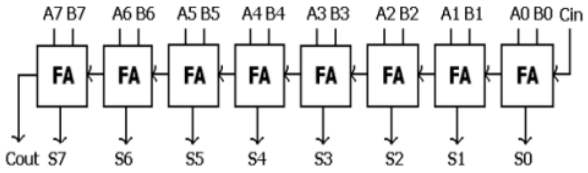

Fig 1: Ripple Carry adder

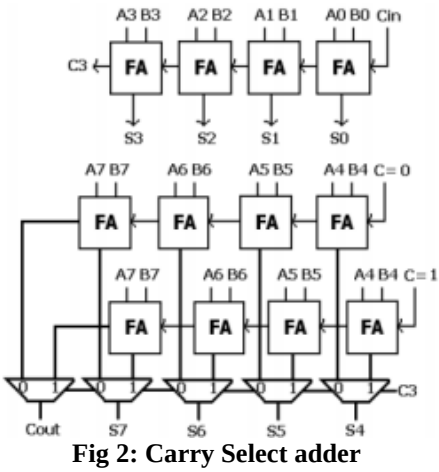

Fig 2: Carry Select adder

- Elimination of inverters in the critical path reduces the switching power. Complex cells reduce the leakage power of the device.

The proposed concept is suitable for any bit widths and at any level of abstractions where the application needs different operating corners by providing the flavours of different adder variants in the same design.

B.RECONFIGURABLE COMPUTING

Reconfigurability is the method which combines the high performance hardware by some flexible software with the use of computing fabrics. In reconfigurable computing there is the possibility of adapting to the hardware during the runtime by the use of new circuit. However the reconfigurability can be viewed with different perspectives viz. the system level and at the functional unit level. The reconfigurable systems are again classified based on their degree of coupling between the functional units and the processing units. These systems may typically contain one or two processors, one or more memories and one or more reconfigurable fabrics.

Secondly the reconfigurable fabrics are again classified into fine grained and coarse grained reconfigurable fabrics. In fine grained reconfigurable fabrics, the bit level reconfigurability will be achieved in the functional units, whereas in coarse grained fabrics, reconfigurability is achieved between the operations of the functional units and also between the entire functional units.

II. CONVENTIAONAL METHOD

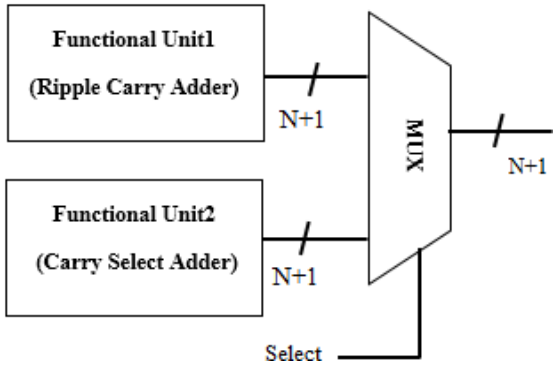

Fig 3: Model diagram of conventional method

The modelled diagram of conventional method of reconfigurable adder architecture is shown in Fig 3 here each functional unit contain one adder architecture. This type of approach will be having higher circuit complexity and also it consumes more area and power. For this reason instead of giving adders to different functional unit, by using shared logic combine the functional unit that means reconfigure the architecture.

Different adder variants are considered as the functionalunits.The combinations of these adder architectures are used todesignthe reconfigurable architectures. Such reconfigurablearchitectures aids in achieving different quality metrics for thedesigns at the system level. For example system level designslike Image processing applications has high priority forperformance and in speech processing of signals have higherpriority for

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power and less priority with its performance.Therefore reconfigurable architectures providing suchflexibilitysave the chip area and power by combining thearchitectures ofboth design constraints. However from thesystem levelperspective, different applications operate at different design constraints, but it is the basic building units operation that brings the difference. Hence in this paper effort has been put to arriveat the reconfigurability with adder architectures, which enables different corners for analysis. The corners like low power, lessarea, high performance can beapproached individually, orcombined or balanced as per the requirement of the applications.

III. PROPOSED METHOD

The proposed concept will enable new corners of optimizationslike "low area - low power" for same performance, "lowestpower", "smallest area" as per the design constraints. It alsoenables new applications for the existing chip architectures.

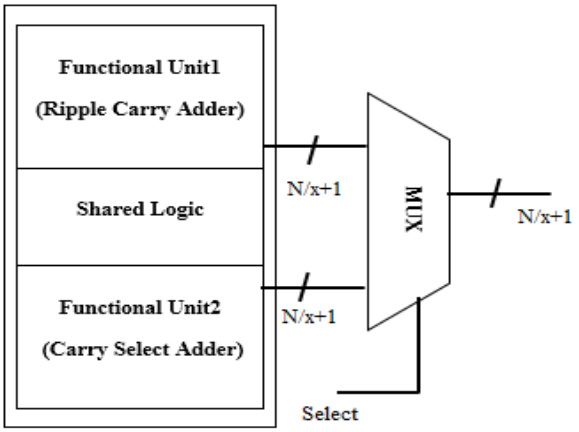

Fig 4: Model diagram of proposed method (shared logic concept)

By exploring the regularity of the adder architectures, the logicsare shared to achieve the reconfigurability in the proposed architectures. Fig 4 shows the abstract view of theproposed reconfigurable adder architectures.

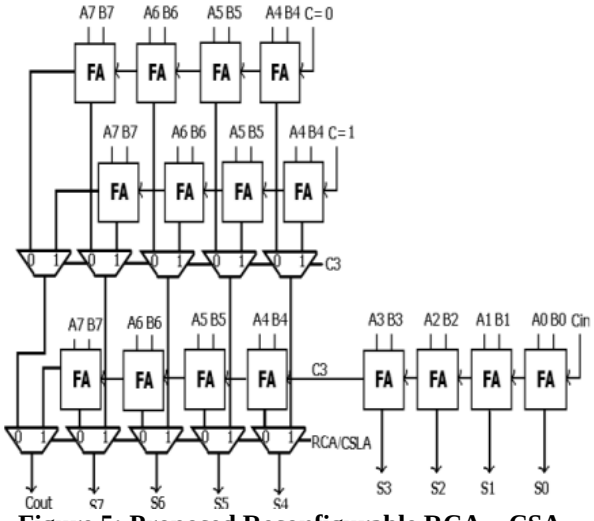

Figure 5: Proposed Reconfigurable RCA – CSA Architecture

In the RCA – CSA combination, the logics of CSA are utilized and RCA isachieved at the cost of some additional multiplexed circuitry to the CSA, and area of complete RCA is saved. This helps in reduced area and reduced power consumption. Proposed RCA–CSA reconfigurable adder is shown in Fig 5All there configurable adder architectures are implemented for 8 bit-widths.

IV. RESULTS

Both the conventional and the proposed reconfigurable architectures are designed and developed in gate level forsynthesis, using the Synopsys Design Compiler EDA tool. The designs were simulated using the Mentor Graphics Model-simsimulator and verified for functionality with the help of waveform editor. The main advantage of resource sharingconcept is to reduce the implementation area; and it was possible due to the merging ofarchitectures between the addervariants. The reduced area will directly impact on the power consumption, as lesser gates areawill lead to lesser switching activity.

As mentioned in the section 3, the shared logicbetween theadder variant's has reduced the area required andalso reduced the power consumption. From this we can provethat the area isone of the factors to reduce the powerconsumption. Regularityin the architectures has made the logicsto be shared and enablesthe flexibility for operation at differentdesign constraints. Thishelps in incorporating thereconfigurable architectures wherethe design supports variousapplications and yields in reduced chip area and powerconsumption. The reduced area will alsoreduce the chip costand fabrication time.

The main advantage of resource sharing concept is toreduce theimplementation area; and it was possible due to the merging ofarchitectures between the adder variants. Thereduced area will directly impact on the power consumption, aslesser gates area will lead to lesser switching activity. Theresults of the proposed approach for the 8-bit reconfigurableadder architectures withthis concept has enabled the design tobe analysed from differentanalysis of corners like less area, low power and comparableperformance. Similar kind of results canbe obtained fordifferent bit widths and more the bit widths more will beopportunity for resource sharing and higher willbe efficiency ofquality metrics. This Concept can be applied at any levels of abstraction.

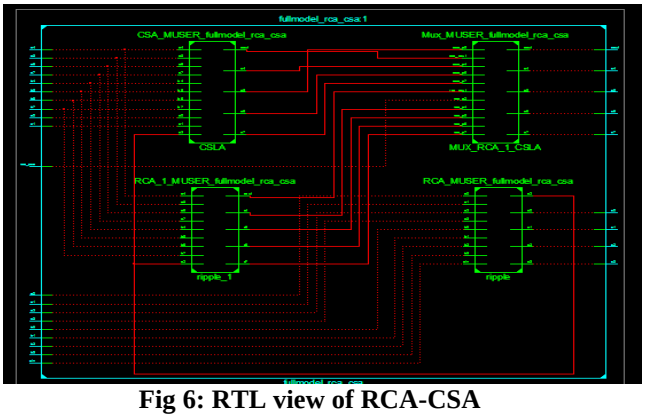

Fig 6: RTL view of RCA-CSA

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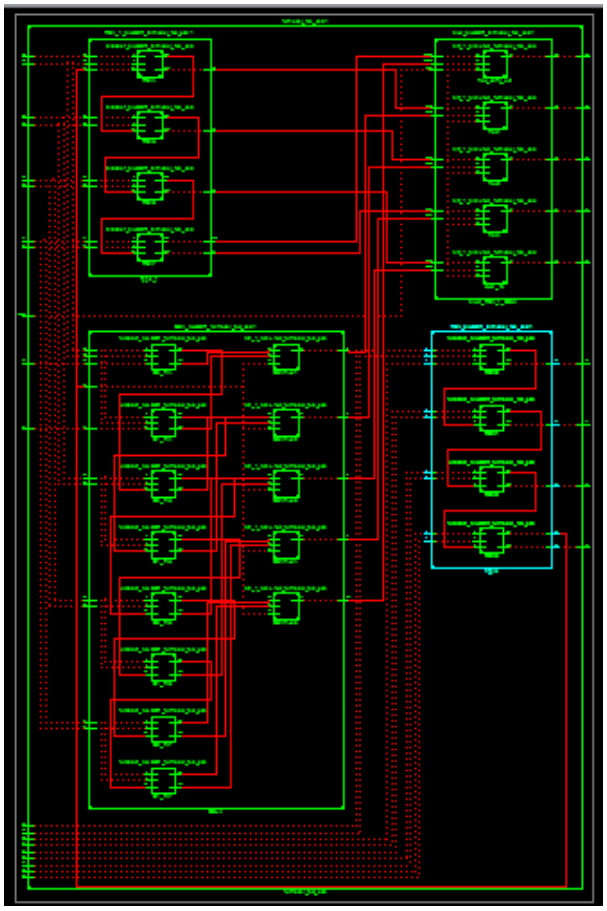

Fig 7: Internal RTL view of RAC-CSA

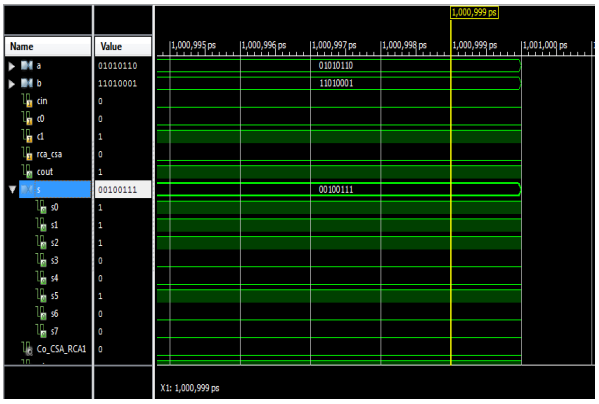

Fig 8: simulation results of RCA-CSA

Table 1: Gate Delay and Net Delay

Total Gate	Delay
logic	22.794ns
route	11.994ns
logic	65.5%
route	34.5%
Total	34.788ns

V.CONCLUSION

A coarse grained reconfigurable fabric is implemented in thispaper; the proposed 8 bit architectures results in 18-54%reduced power consumption when designed with differentcombination of reconfigurable adder architectures and alsoaccounted for 14-44% of area reduction. Thepartitioned multiplex concept has reduced the area and therebydirectly reduces the power consumption of the design. Theproposed reconfigurable architectures can be utilized where theapplication needs ultra-low power in terms of leakage, highperformance, low area, and a balanced design quality metrics.Further carrying this reconfigurability in to the system levelwillimpact the same way and helps in accommodating all addervariants within the same/reduced area of the regulararchitecture.These architectures are pervasive and can beimplemented atvarious levels of hierarchical abstractions.

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